1. A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a metal layer overlying said semiconductor substrate;

etching through said metal layer to form connective lines;

thereafter etching partially through said metal layer to form vias;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

2. The method according to Claim 1 wherein said metal layer comprises one of the group of: aluminum, aluminum alloys, tungsten and copper.

3. The method according to Claim 1 wherein said semiconductor substrate comprises semiconductor devices in and on a silicon substrate covered by an insulating layer.

4. The method according to Claim 1 wherein said step of etching partially through said metal layer to form vias comprises a timed etch.

5. The method according to Claim 1 wherein said dielectric layer comprises one of the group of: SiO_2, SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), and VT-4 (tetrafluoro-p-xylylene).

6. The method according to Claim 1 wherein said dielectric layer is deposited to a thickness of between about 5,000 Angstroms and 20,000 Angstroms.

7. The method according to Claim 1 further comprising depositing an anti-reflective coating layer overlying said metal layer prior to said step of etching through said metal layer to form connective lines.

8. The method according to Claim 7 wherein said

anti-reflective coating layer comprises titanium nitride (TiN) and wherein said anti-reflective coating layer is a polishing stop for said step of polishing down said dielectric layer.

9. A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing a second metal layer overlying said first metal layer;

depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;

etching through said anti-reflective coating layer, said second metal layer, and said first metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of

20 the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

10. The method according to Claim 9 wherein said first metal layer and said second metal layer comprise one of the group of: : aluminum, aluminum alloys, tungsten and copper.

11. The method according to Claim 9 wherein said first metal layer is deposited to a thickness of between about 1,000 Angstroms and 10,000 Angstroms.

12. The method according to Claim 9 wherein said second metal layer is deposited to a thickness of between about 3,000 Angstroms and 10,000 Angstroms.

13. The method according to Claim 9 wherein said step of etching through said ARC layer and said second metal layer to form vias comprises a timed etch.

14. The method according to Claim 9 further comprising depositing an etch stop layer after said step of depositing a first metal layer and before said step of depositing a second metal layer.

15. The method according to Claim 14 wherein said step of etching through said ARC layer and said second metal layer to form vias has an endpoint at said etch stop layer.

16. The method according to Claim 14 wherein said etch stop layer comprises one of the group of: titanium nitride (TiN), titanium (T), tungsten (W), tungsten nitride (WN), tantalum (Ta), and tantalum nitride (TaN).

17. The method according to Claim 9 wherein said dielectric layer comprises one of the group of: SiO_2, SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), and VT-4 (tetrafluoro-p-xylylene).

18. A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer;

depositing a second metal layer overlying said first metal layer;

depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;

etching through said anti-reflective coating layer, said second metal layer, said etch stop layer, and said second metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias wherein said etch stop layer acts as an etch stop;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

19. The method according to Claim 18 wherein said first metal layer and said second metal layer comprise one of the group of: aluminum, aluminum alloys, tungsten, and copper.

20. The method according to Claim 18 wherein said first

metal layer is deposited to a thickness of between about 1,000 Angstroms and 10,000 Angstroms.

21. The method according to Claim 18 wherein said second metal layer is deposited to a thickness of between about 3,000 Angstroms and 10,000 Angstroms.

22. The method according to Claim 18 wherein said etch stop layer comprises one of the group of: titanium nitride (TiN), titanium (T), tungsten (W), tungsten nitride (WN), tantalum (Ta), and tantalum nitride (TaN).

23. The method according to Claim 18 wherein said dielectric layer comprises one of the group of: SiO_2, SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), and VT-4 (tetrafluoro-p-xylylene).